#-----------------------------------------------------------

# Vivado v2018.3 (64-bit)

# SW Build 2405991 on Thu Dec 6 23:38:27 MST 2018

# IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

# Start of session at: Wed Oct 16 15:22:56 2024

# Process ID: 28108

# Current directory: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7\_100t/hello\_world\_arty\_a7\_100t.runs/synth\_1

# Command line: vivado.exe -log hello\_world\_arty\_a7.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source hello\_world\_arty\_a7.tcl

# Log file: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7\_100t/hello\_world\_arty\_a7\_100t.runs/synth\_1/hello\_world\_arty\_a7.vds

# Journal file: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7\_100t/hello\_world\_arty\_a7\_100t.runs/synth\_1\vivado.jou

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source hello\_world\_arty\_a7.tcl -notrace

Command: synth\_design -top hello\_world\_arty\_a7 -part xc7a100ticsg324-1L

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100ti'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100ti'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 37360

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Starting RTL Elaboration : Time (s): cpu = 00:00:00 ; elapsed = 00:00:01 . Memory (MB): peak = 431.664 ; gain = 99.523

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INFO: [Synth 8-6157] synthesizing module 'hello\_world\_arty\_a7' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_mcu' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel\_mcu.v:8]

Parameter CLOCK\_FREQUENCY bound to: 50000000 - type: integer

Parameter UART\_BAUD\_RATE bound to: 9600 - type: integer

Parameter MEMORY\_SIZE bound to: 8192 - type: integer

Parameter MEMORY\_INIT\_FILE bound to: hello\_world.hex - type: string

Parameter BOOT\_ADDRESS bound to: 0 - type: integer

Parameter GPIO\_WIDTH bound to: 1 - type: integer

Parameter SPI\_NUM\_CHIP\_SELECT bound to: 1 - type: integer

Parameter NUM\_DEVICES bound to: 5 - type: integer

Parameter D0\_RAM bound to: 0 - type: integer

Parameter D1\_UART bound to: 1 - type: integer

Parameter D2\_MTIMER bound to: 2 - type: integer

Parameter D3\_GPIO bound to: 3 - type: integer

Parameter D4\_SPI bound to: 4 - type: integer

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_core' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel\_core.v:8]

Parameter BOOT\_ADDRESS bound to: 0 - type: integer

Parameter MARCHID bound to: 12'b111100010010

Parameter MIMPID bound to: 12'b111100010011

Parameter CYCLE bound to: 12'b110000000000

Parameter TIME bound to: 12'b110000000001

Parameter INSTRET bound to: 12'b110000000010

Parameter CYCLEH bound to: 12'b110010000000

Parameter TIMEH bound to: 12'b110010000001

Parameter INSTRETH bound to: 12'b110010000010

Parameter MSTATUS bound to: 12'b001100000000

Parameter MSTATUSH bound to: 12'b001100010000

Parameter MISA bound to: 12'b001100000001

Parameter MIE bound to: 12'b001100000100

Parameter MTVEC bound to: 12'b001100000101

Parameter MSCRATCH bound to: 12'b001101000000

Parameter MEPC bound to: 12'b001101000001

Parameter MCAUSE bound to: 12'b001101000010

Parameter MTVAL bound to: 12'b001101000011

Parameter MIP bound to: 12'b001101000100

Parameter MCYCLE bound to: 12'b101100000000

Parameter MINSTRET bound to: 12'b101100000010

Parameter MCYCLEH bound to: 12'b101110000000

Parameter MINSTRETH bound to: 12'b101110000010

Parameter WB\_ALU bound to: 3'b000

Parameter WB\_LOAD\_UNIT bound to: 3'b001

Parameter WB\_UPPER\_IMM bound to: 3'b010

Parameter WB\_TARGET\_ADDER bound to: 3'b011

Parameter WB\_CSR bound to: 3'b100

Parameter WB\_PC\_PLUS\_4 bound to: 3'b101

Parameter I\_TYPE\_IMMEDIATE bound to: 3'b001

Parameter S\_TYPE\_IMMEDIATE bound to: 3'b010

Parameter B\_TYPE\_IMMEDIATE bound to: 3'b011

Parameter U\_TYPE\_IMMEDIATE bound to: 3'b100

Parameter J\_TYPE\_IMMEDIATE bound to: 3'b101

Parameter CSR\_TYPE\_IMMEDIATE bound to: 3'b110

Parameter PC\_BOOT bound to: 2'b00

Parameter PC\_EPC bound to: 2'b01

Parameter PC\_TRAP bound to: 2'b10

Parameter PC\_NEXT bound to: 2'b11

Parameter LOAD\_SIZE\_BYTE bound to: 2'b00

Parameter LOAD\_SIZE\_HALF bound to: 2'b01

Parameter LOAD\_SIZE\_WORD bound to: 2'b10

Parameter CSR\_RWX bound to: 2'b01

Parameter CSR\_RSX bound to: 2'b10

Parameter CSR\_RCX bound to: 2'b11

Parameter STATE\_RESET bound to: 4'b0001

Parameter STATE\_OPERATING bound to: 4'b0010

Parameter STATE\_TRAP\_TAKEN bound to: 4'b0100

Parameter STATE\_TRAP\_RETURN bound to: 4'b1000

Parameter NOP\_INSTRUCTION bound to: 19 - type: integer

Parameter OPCODE\_OP bound to: 7'b0110011

Parameter OPCODE\_OP\_IMM bound to: 7'b0010011

Parameter OPCODE\_LOAD bound to: 7'b0000011

Parameter OPCODE\_STORE bound to: 7'b0100011

Parameter OPCODE\_BRANCH bound to: 7'b1100011

Parameter OPCODE\_JAL bound to: 7'b1101111

Parameter OPCODE\_JALR bound to: 7'b1100111

Parameter OPCODE\_LUI bound to: 7'b0110111

Parameter OPCODE\_AUIPC bound to: 7'b0010111

Parameter OPCODE\_MISC\_MEM bound to: 7'b0001111

Parameter OPCODE\_SYSTEM bound to: 7'b1110011

Parameter FUNCT3\_ADD bound to: 3'b000

Parameter FUNCT3\_SUB bound to: 3'b000

Parameter FUNCT3\_SLT bound to: 3'b010

Parameter FUNCT3\_SLTU bound to: 3'b011

Parameter FUNCT3\_AND bound to: 3'b111

Parameter FUNCT3\_OR bound to: 3'b110

Parameter FUNCT3\_XOR bound to: 3'b100

Parameter FUNCT3\_SLL bound to: 3'b001

Parameter FUNCT3\_SRL bound to: 3'b101

Parameter FUNCT3\_SRA bound to: 3'b101

Parameter FUNCT3\_ADDI bound to: 3'b000

Parameter FUNCT3\_SLTI bound to: 3'b010

Parameter FUNCT3\_SLTIU bound to: 3'b011

Parameter FUNCT3\_ANDI bound to: 3'b111

Parameter FUNCT3\_ORI bound to: 3'b110

Parameter FUNCT3\_XORI bound to: 3'b100

Parameter FUNCT3\_SLLI bound to: 3'b001

Parameter FUNCT3\_SRLI bound to: 3'b101

Parameter FUNCT3\_SRAI bound to: 3'b101

Parameter FUNCT3\_BEQ bound to: 3'b000

Parameter FUNCT3\_BNE bound to: 3'b001

Parameter FUNCT3\_BLT bound to: 3'b100

Parameter FUNCT3\_BGE bound to: 3'b101

Parameter FUNCT3\_BLTU bound to: 3'b110

Parameter FUNCT3\_BGEU bound to: 3'b111

Parameter FUNCT3\_SB bound to: 3'b000

Parameter FUNCT3\_SH bound to: 3'b001

Parameter FUNCT3\_SW bound to: 3'b010

Parameter FUNCT3\_ECALL bound to: 3'b000

Parameter FUNCT3\_EBREAK bound to: 3'b000

Parameter FUNCT3\_MRET bound to: 3'b000

Parameter FUNCT7\_SUB bound to: 7'b0100000

Parameter FUNCT7\_SRA bound to: 7'b0100000

Parameter FUNCT7\_ADD bound to: 7'b0000000

Parameter FUNCT7\_SLT bound to: 7'b0000000

Parameter FUNCT7\_SLTU bound to: 7'b0000000

Parameter FUNCT7\_AND bound to: 7'b0000000

Parameter FUNCT7\_OR bound to: 7'b0000000

Parameter FUNCT7\_XOR bound to: 7'b0000000

Parameter FUNCT7\_SLL bound to: 7'b0000000

Parameter FUNCT7\_SRL bound to: 7'b0000000

Parameter FUNCT7\_SRAI bound to: 7'b0100000

Parameter FUNCT7\_SLLI bound to: 7'b0000000

Parameter FUNCT7\_SRLI bound to: 7'b0000000

Parameter FUNCT7\_ECALL bound to: 7'b0000000

Parameter FUNCT7\_EBREAK bound to: 7'b0000000

Parameter FUNCT7\_MRET bound to: 7'b0011000

Parameter RS1\_ECALL bound to: 5'b00000

Parameter RS1\_EBREAK bound to: 5'b00000

Parameter RS1\_MRET bound to: 5'b00000

Parameter RS2\_ECALL bound to: 5'b00000

Parameter RS2\_EBREAK bound to: 5'b00001

Parameter RS2\_MRET bound to: 5'b00010

Parameter RD\_ECALL bound to: 5'b00000

Parameter RD\_EBREAK bound to: 5'b00000

Parameter RD\_MRET bound to: 5'b00000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_core' (1#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel\_core.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_bus' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/bus/rvsteel\_bus.v:8]

Parameter NUM\_DEVICES bound to: 5 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_bus' (2#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/bus/rvsteel\_bus.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_ram' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel\_ram.v:8]

Parameter MEMORY\_SIZE bound to: 8192 - type: integer

Parameter MEMORY\_INIT\_FILE bound to: hello\_world.hex - type: string

INFO: [Synth 8-3876] $readmem data file 'hello\_world.hex' is read successfully [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel\_ram.v:53]

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_ram' (3#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel\_ram.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_uart' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/uart/rvsteel\_uart.v:8]

Parameter CLOCK\_FREQUENCY bound to: 50000000 - type: integer

Parameter UART\_BAUD\_RATE bound to: 9600 - type: integer

Parameter CYCLES\_PER\_BAUD bound to: 5208 - type: integer

Parameter REG\_WDATA bound to: 5'b00000

Parameter REG\_RDATA bound to: 5'b00100

Parameter REG\_READY bound to: 5'b01000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_uart' (4#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/uart/rvsteel\_uart.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_mtimer' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mtimer/rvsteel\_mtimer.v:8]

Parameter REG\_ADDR\_WIDTH bound to: 2'b11

Parameter REG\_CR bound to: 3'b000

Parameter REG\_MTIMEL bound to: 3'b001

Parameter REG\_MTIMEH bound to: 3'b010

Parameter REG\_MTIMECMPL bound to: 3'b011

Parameter REG\_MTIMECMPH bound to: 3'b100

Parameter BIT\_CR\_EN bound to: 5'b00000

Parameter BIT\_CR\_WIDTH bound to: 5'b00001

Parameter CR\_PADDING bound to: 31'b0000000000000000000000000000000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_mtimer' (5#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mtimer/rvsteel\_mtimer.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_gpio' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/gpio/rvsteel\_gpio.v:8]

Parameter GPIO\_WIDTH bound to: 1 - type: integer

Parameter REG\_ADDR\_WIDTH bound to: 2'b11

Parameter REG\_IN bound to: 3'b000

Parameter REG\_OE bound to: 3'b001

Parameter REG\_OUT bound to: 3'b010

Parameter REG\_CLR bound to: 3'b011

Parameter REG\_SET bound to: 3'b100

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_gpio' (6#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/gpio/rvsteel\_gpio.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel\_spi' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/spi/rvsteel\_spi.v:8]

Parameter SPI\_NUM\_CHIP\_SELECT bound to: 1 - type: integer

Parameter SPI\_READY bound to: 4'b0001

Parameter SPI\_IDLE bound to: 4'b0010

Parameter SPI\_CPOL bound to: 4'b0100

Parameter SPI\_CPOL\_N bound to: 4'b1000

Parameter REG\_CPOL bound to: 5'b00000

Parameter REG\_CPHA bound to: 5'b00100

Parameter REG\_CHIP\_SELECT bound to: 5'b01000

Parameter REG\_CLOCK\_CONF bound to: 5'b01100

Parameter REG\_WDATA bound to: 5'b10000

Parameter REG\_RDATA bound to: 5'b10100

Parameter REG\_BUSY bound to: 5'b11000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_spi' (7#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/spi/rvsteel\_spi.v:8]

INFO: [Synth 8-6155] done synthesizing module 'rvsteel\_mcu' (8#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel\_mcu.v:8]

INFO: [Synth 8-6155] done synthesizing module 'hello\_world\_arty\_a7' (9#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7.v:8]

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Finished RTL Elaboration : Time (s): cpu = 00:00:00 ; elapsed = 00:00:03 . Memory (MB): peak = 496.117 ; gain = 163.977

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

WARNING: [Synth 8-3295] tying undriven pin rvsteel\_mcu\_instance:uart\_rx to constant 0 [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7.v:34]

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:00 ; elapsed = 00:00:03 . Memory (MB): peak = 496.117 ; gain = 163.977

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:00 ; elapsed = 00:00:03 . Memory (MB): peak = 496.117 ; gain = 163.977

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INFO: [Device 21-403] Loading part xc7a100ticsg324-1L

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7\_constraints.xdc]

Finished Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7\_constraints.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7\_constraints.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/hello\_world\_arty\_a7\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/hello\_world\_arty\_a7\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 863.000 ; gain = 0.000

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 863.000 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 863.000 ; gain = 0.000

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.006 . Memory (MB): peak = 863.000 ; gain = 0.000

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Finished Constraint Validation : Time (s): cpu = 00:00:02 ; elapsed = 00:00:11 . Memory (MB): peak = 863.000 ; gain = 530.859

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Start Loading Part and Timing Information

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Loading part: xc7a100ticsg324-1L

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:02 ; elapsed = 00:00:11 . Memory (MB): peak = 863.000 ; gain = 530.859

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:02 ; elapsed = 00:00:11 . Memory (MB): peak = 863.000 ; gain = 530.859

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INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel\_core.v:1341]

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel\_core.v:1339]

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel\_core.v:1630]

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel\_core.v:459]

INFO: [Synth 8-802] inferred FSM for state register 'current\_state\_reg' in module 'rvsteel\_core'

INFO: [Synth 8-5546] ROM "integer\_file\_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "program\_counter\_source" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_mstatus\_mpie" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_mcause" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next\_state" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5546] ROM "integer\_file\_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer\_file\_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "program\_counter\_source" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_mstatus\_mpie" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_mcause" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next\_state" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_mepc" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_mtvec" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx\_data0" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx\_data0" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "tx\_bit\_counter" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx\_bit\_counter" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx\_bit\_counter0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "read\_data" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-802] inferred FSM for state register 'curr\_state\_reg' in module 'rvsteel\_spi'

INFO: [Synth 8-5545] ROM "cs0" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5544] ROM "next\_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next\_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next\_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next\_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

---------------------------------------------------------------------------------------------------

State | New Encoding | Previous Encoding

---------------------------------------------------------------------------------------------------

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STATE\_RESET | 0001 | 0001

STATE\_OPERATING | 0010 | 0010

STATE\_TRAP\_TAKEN | 0100 | 0100

STATE\_TRAP\_RETURN | 1000 | 1000

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INFO: [Synth 8-3898] No Re-encoding of one hot register 'current\_state\_reg' in module 'rvsteel\_core'

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State | New Encoding | Previous Encoding

---------------------------------------------------------------------------------------------------

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SPI\_READY | 0001 | 0001

SPI\_CPOL | 0100 | 0100

SPI\_CPOL\_N | 1000 | 1000

SPI\_IDLE | 0010 | 0010

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INFO: [Synth 8-3898] No Re-encoding of one hot register 'curr\_state\_reg' in module 'rvsteel\_spi'

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:12 . Memory (MB): peak = 863.000 ; gain = 530.859

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 64 Bit Adders := 4

3 Input 32 Bit Adders := 1

2 Input 32 Bit Adders := 8

2 Input 8 Bit Adders := 1

2 Input 4 Bit Adders := 3

+---XORs :

2 Input 32 Bit XORs := 1

2 Input 1 Bit XORs := 3

+---Registers :

64 Bit Registers := 5

32 Bit Registers := 46

16 Bit Registers := 2

10 Bit Registers := 1

8 Bit Registers := 7

5 Bit Registers := 2

4 Bit Registers := 4

1 Bit Registers := 40

+---RAMs :

64K Bit RAMs := 1

+---Muxes :

2 Input 64 Bit Muxes := 11

2 Input 32 Bit Muxes := 85

4 Input 32 Bit Muxes := 23

23 Input 32 Bit Muxes := 1

6 Input 32 Bit Muxes := 1

7 Input 32 Bit Muxes := 1

2 Input 31 Bit Muxes := 2

2 Input 24 Bit Muxes := 1

2 Input 16 Bit Muxes := 2

2 Input 10 Bit Muxes := 2

4 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 2

8 Input 5 Bit Muxes := 1

25 Input 5 Bit Muxes := 1

2 Input 5 Bit Muxes := 1

26 Input 5 Bit Muxes := 1

5 Input 4 Bit Muxes := 4

2 Input 4 Bit Muxes := 26

4 Input 4 Bit Muxes := 5

3 Input 4 Bit Muxes := 4

7 Input 3 Bit Muxes := 3

3 Input 3 Bit Muxes := 1

2 Input 3 Bit Muxes := 2

2 Input 2 Bit Muxes := 4

5 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 76

19 Input 1 Bit Muxes := 1

6 Input 1 Bit Muxes := 8

3 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 6

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module hello\_world\_arty\_a7

Detailed RTL Component Info :

+---Registers :

1 Bit Registers := 2

Module rvsteel\_core

Detailed RTL Component Info :

+---Adders :

2 Input 64 Bit Adders := 3

3 Input 32 Bit Adders := 1

2 Input 32 Bit Adders := 3

+---XORs :

2 Input 32 Bit XORs := 1

2 Input 1 Bit XORs := 2

+---Registers :

64 Bit Registers := 3

32 Bit Registers := 41

16 Bit Registers := 2

5 Bit Registers := 1

4 Bit Registers := 1

1 Bit Registers := 13

+---Muxes :

2 Input 64 Bit Muxes := 9

2 Input 32 Bit Muxes := 79

4 Input 32 Bit Muxes := 22

23 Input 32 Bit Muxes := 1

2 Input 31 Bit Muxes := 2

2 Input 24 Bit Muxes := 1

2 Input 16 Bit Muxes := 2

4 Input 8 Bit Muxes := 1

8 Input 5 Bit Muxes := 1

25 Input 5 Bit Muxes := 1

2 Input 5 Bit Muxes := 1

26 Input 5 Bit Muxes := 1

5 Input 4 Bit Muxes := 1

2 Input 4 Bit Muxes := 8

4 Input 4 Bit Muxes := 4

7 Input 3 Bit Muxes := 2

2 Input 2 Bit Muxes := 4

5 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 48

19 Input 1 Bit Muxes := 1

6 Input 1 Bit Muxes := 1

3 Input 1 Bit Muxes := 1

Module rvsteel\_bus

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 5

+---Registers :

5 Bit Registers := 1

+---Muxes :

2 Input 1 Bit Muxes := 1

Module rvsteel\_ram

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 1

1 Bit Registers := 3

+---RAMs :

64K Bit RAMs := 1

+---Muxes :

2 Input 32 Bit Muxes := 6

2 Input 8 Bit Muxes := 1

Module rvsteel\_uart

Detailed RTL Component Info :

+---Adders :

2 Input 4 Bit Adders := 2

+---Registers :

32 Bit Registers := 1

10 Bit Registers := 1

8 Bit Registers := 2

4 Bit Registers := 2

1 Bit Registers := 5

+---Muxes :

4 Input 32 Bit Muxes := 1

2 Input 10 Bit Muxes := 2

2 Input 8 Bit Muxes := 1

5 Input 4 Bit Muxes := 1

3 Input 4 Bit Muxes := 1

2 Input 4 Bit Muxes := 6

4 Input 4 Bit Muxes := 1

3 Input 3 Bit Muxes := 1

2 Input 1 Bit Muxes := 14

Module rvsteel\_mtimer

Detailed RTL Component Info :

+---Adders :

2 Input 64 Bit Adders := 1

+---Registers :

64 Bit Registers := 2

32 Bit Registers := 1

1 Bit Registers := 4

+---Muxes :

2 Input 64 Bit Muxes := 2

6 Input 1 Bit Muxes := 6

2 Input 1 Bit Muxes := 2

Module rvsteel\_gpio

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 1

1 Bit Registers := 4

+---Muxes :

6 Input 32 Bit Muxes := 1

6 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 4

2 Input 1 Bit Muxes := 4

Module rvsteel\_spi

Detailed RTL Component Info :

+---Adders :

2 Input 8 Bit Adders := 1

2 Input 4 Bit Adders := 1

+---XORs :

2 Input 1 Bit XORs := 1

+---Registers :

32 Bit Registers := 1

8 Bit Registers := 5

4 Bit Registers := 1

1 Bit Registers := 9

+---Muxes :

7 Input 32 Bit Muxes := 1

3 Input 4 Bit Muxes := 3

2 Input 4 Bit Muxes := 12

5 Input 4 Bit Muxes := 2

2 Input 3 Bit Muxes := 2

7 Input 3 Bit Muxes := 1

2 Input 1 Bit Muxes := 7

5 Input 1 Bit Muxes := 2

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-5544] ROM "csr\_mcause" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "p\_0\_out" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr\_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx\_data0" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5545] ROM "cs0" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-3333] propagating constant 1 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/tx\_register\_reg[9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[6]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[34] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[2] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[36] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[4] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[37] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[5] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[38] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[6] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[40] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[8] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[41] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[42] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[10] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[44] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[45] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[13] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[46] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[47] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[15] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[32] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[0] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[33] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[0] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[43] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[11] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[39] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[7] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[35] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[3] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[48] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[16] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[49] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[17] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[50] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[18] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[51] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[19] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[52] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[20] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[53] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[21] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[54] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[22] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[55] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[23] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[56] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[24] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[57] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[25] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[58] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[26] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[59] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[27] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[60] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[28] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[61] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[29] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[62] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[30] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[63] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_utime\_reg[31] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mtvec\_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[30]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[28]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[30]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[28]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[29]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[28]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[29]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[27]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[29]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[24]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[27]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[27]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[31]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[26]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[31]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[26]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[26]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[25]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[26]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[25]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[25]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[21]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[25]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[23]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[21]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[23]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[21]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[23]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[23]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[24]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[23]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[19]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[24]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[22]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[24]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[22]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[22]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[20]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[22]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[20]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[20]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[19]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[20]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[17]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[19]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[18]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[19]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[18]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[18]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[17]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[18]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[16]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[17]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[15]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[17]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[14]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[15]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[16]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[15]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[16]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[16]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[11]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[16]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[11]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[10]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[11]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[10]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[9]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[10]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[9]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[8]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[9]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[8]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[8]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[14]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[13]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[14]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[13]' (FDS) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[12]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[14]' (FDR) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[12]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/read\_data\_reg[14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/read\_data\_reg[12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /csr\_mip\_meip\_reg)

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /csr\_mip\_msip\_reg)

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[2] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[3] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[4] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[5] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[6] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[7] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[8] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[10] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[11] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[13] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_core\_instance /\csr\_mip\_mfip\_reg[15] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[5]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[7]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[6]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[0]' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[2]' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[4]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[6]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[5]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[1]' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[3]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[3] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[5]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[4]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[4]' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[3]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[7]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[3]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[2]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[0]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[2]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[3]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[4]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[3] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_register\_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[1]' (FDRE) to 'rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_data\_reg[0]'

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[3]' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[5]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[5] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[5]' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[6]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[6] )

INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[6]' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[7]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel\_mcu\_instance/rvsteel\_spi\_instance/rx\_reg\_reg[7] )

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:30 ; elapsed = 00:02:09 . Memory (MB): peak = 938.801 ; gain = 606.660

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Start ROM, RAM, DSP and Shift Register Reporting

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Block RAM: Preliminary Mapping Report (see note below)

+-------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

|Module Name | RTL Object | PORT A (Depth x Width) | W | R | PORT B (Depth x Width) | W | R | Ports driving FF | RAMB18 | RAMB36 |

+-------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

|rvsteel\_ram: | ram\_reg | 2 K x 32(READ\_FIRST) | W | | 2 K x 32(WRITE\_FIRST) | | R | Port A and B | 0 | 2 |

+-------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

Note: The table above is a preliminary report that shows the Block RAMs at the current stage of the synthesis flow. Some Block RAMs may be reimplemented as non Block RAM primitives later in the synthesis flow. Multiple instantiated Block RAMs are reported only once.

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Finished ROM, RAM, DSP and Shift Register Reporting

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INFO: [Synth 8-6837] The timing for the instance i\_1/rvsteel\_mcu\_instance/rvsteel\_ram\_instance/ram\_reg\_0 (implemented as a Block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

INFO: [Synth 8-6837] The timing for the instance i\_1/rvsteel\_mcu\_instance/rvsteel\_ram\_instance/ram\_reg\_1 (implemented as a Block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:33 ; elapsed = 00:02:15 . Memory (MB): peak = 938.801 ; gain = 606.660

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:40 ; elapsed = 00:02:33 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start ROM, RAM, DSP and Shift Register Reporting

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Block RAM: Final Mapping Report

+-------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

|Module Name | RTL Object | PORT A (Depth x Width) | W | R | PORT B (Depth x Width) | W | R | Ports driving FF | RAMB18 | RAMB36 |

+-------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

|rvsteel\_ram: | ram\_reg | 2 K x 32(READ\_FIRST) | W | | 2 K x 32(WRITE\_FIRST) | | R | Port A and B | 0 | 2 |

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Finished ROM, RAM, DSP and Shift Register Reporting

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

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+-+--------------+------------+----------+

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Start Technology Mapping

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INFO: [Synth 8-3886] merging instance 'rvsteel\_mcu\_instance/rvsteel\_ram\_instance/reset\_reg\_reg' (FD) to 'rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_reg\_reg'

INFO: [Synth 8-6837] The timing for the instance rvsteel\_mcu\_instance/rvsteel\_ram\_instance/ram\_reg\_0 (implemented as a Block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

INFO: [Synth 8-6837] The timing for the instance rvsteel\_mcu\_instance/rvsteel\_ram\_instance/ram\_reg\_1 (implemented as a Block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

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Finished Technology Mapping : Time (s): cpu = 00:00:43 ; elapsed = 00:02:42 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----------+------+

| |Cell |Count |

+------+-----------+------+

|1 |BUFG | 2|

|2 |CARRY4 | 158|

|3 |LUT1 | 11|

|4 |LUT2 | 94|

|5 |LUT3 | 263|

|6 |LUT4 | 416|

|7 |LUT5 | 584|

|8 |LUT6 | 1270|

|9 |MUXF7 | 339|

|10 |RAMB36E1 | 1|

|11 |RAMB36E1\_1 | 1|

|12 |FDRE | 1680|

|13 |FDSE | 88|

|14 |IBUF | 2|

|15 |OBUF | 1|

+------+-----------+------+

Report Instance Areas:

+------+----------------------------+---------------+------+

| |Instance |Module |Cells |

+------+----------------------------+---------------+------+

|1 |top | | 4910|

|2 | rvsteel\_mcu\_instance |rvsteel\_mcu | 4902|

|3 | rvsteel\_bus\_instance |rvsteel\_bus | 84|

|4 | rvsteel\_core\_instance |rvsteel\_core | 4336|

|5 | rvsteel\_gpio\_instance |rvsteel\_gpio | 5|

|6 | rvsteel\_mtimer\_instance |rvsteel\_mtimer | 253|

|7 | rvsteel\_ram\_instance |rvsteel\_ram | 4|

|8 | rvsteel\_spi\_instance |rvsteel\_spi | 94|

|9 | rvsteel\_uart\_instance |rvsteel\_uart | 124|

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:42 ; elapsed = 00:02:38 . Memory (MB): peak = 1157.637 ; gain = 458.613

Synthesis Optimization Complete : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 1157.637 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

305 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:44 ; elapsed = 00:02:46 . Memory (MB): peak = 1157.637 ; gain = 838.520

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1157.637 ; gain = 0.000

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7\_100t/hello\_world\_arty\_a7\_100t.runs/synth\_1/hello\_world\_arty\_a7.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file hello\_world\_arty\_a7\_utilization\_synth.rpt -pb hello\_world\_arty\_a7\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Wed Oct 16 15:25:47 2024...